1.1. Overview

This Module, type CBD 8210, is a double height VME card allowing a CAMAC Branch (EUR 4600) to be driven from VME. This means that up to 7 CAMAC crates, on the same branch highway, can be accessed from VME. The use of PALs and I.C.s in the mechanical SO format makes it a high performance module. The design of this module has been made with the intention of allowing it to work in conjunction with a second module enabling DMA transfers to be made from CAMAC to VME.

The module is an update of the CAMAC Branch Driving VME module developed by the French Research Institute at SACLAY. The characteristics are the following:

a) Programmable 16-bit or 24-bit transfers.
b) Two external interrupts with handshake.
c) Comprehensive LAM handling.
d) Addition of a DMA module at a later date.
e) Complete monitoring of all transfers displayed on the front panel.
f) Multi-crate addressing possible.

1.2. Address Mapping

The mapping of the CAMAC address field has been taken from the CERN publication "CERN IMPLEMENTATION RECOMMENDATION for MC 68000 BASED CAMAC PORT CONTROLLERS'. Therefore, for the 24-bit address of VME the following bit allocation exists:

Bits <23..22>	=	1..0
Bits <21..19>	=	Branch address (0 to 7 = 8 branches)
Bits <18..16>	=	Crate address 1 - 7 standard addressing.
Bits <15..11>	=	N address - CAMAC station number
Bits <10..07>	=	A address - CAMAC sub-address
Bits <06..02>	=	F code - CAMAC function
Bit <01>	=	CAMAC Word length 0 = 24-bit 1 = 16-bit

Thus all the CAMAC system parameters are mapped onto the VME address field.

The CBD 8210 can only drive one CAMAC branch where the number of the branch to be driven is selected by a front panel switch.

In practice, when a cycle of 24 bits is to be carried out, the master effects a first cycle with AD01 = 0 (detection of a 24-bit cycle) followed by a cycle with AD01 = 1 allowing the utilization of the instructions 'LWORD' of the MC 68000.

1.3. Selection of Internal Registers

The internal registers are selected by using the command CR0 N29. They are as follows:

CSR	:	CR0 N29 A0 F0	Read/Write	
ITF	:	CR0 N29 A0 F4	Write	
INT. CONT.1	:	CR0 N29 A0 F5	Read/Write	Control
INT. CONT.1	:	CR0 N29 A0 F1	Read/Write	Data
INT. CONT.2	:	CR0 N29 A0 F6	Read/Write	
INT. CONT.2	:	CR0 N29 A0 F2	Read/Write	
INT. CONT.3	:	CR0 N29 A0 F7	Read/Write	
INT. CONT.3	:	CR0 N29 A0 F3	Read/Write	
CAR	:	CR0 N29 A0 F8	Read/Write	
BTB	:	CR0 N29 A0 F9	Read	
BZ	:	CR0 N29 A0 F9	Write	
GL	:	CR0 N29 A0 F10	Read	